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Subject : TechnoTrend PCline budget family information

Revision overview

Revision/Date	Author	Description
20021230	MM	Initial draft.
20030524	MM	Updated. Added infrared section.
20030526	MM	Added transport data stream interface communication between BSRU6-701A and SAA7146A. Added information from Philips reference design 'Sylt'. Added system overview. Added EEPROM section.
20030614	MM	Updated common interface section. Added table of contents.
20030704	MM	Added common interface chapter.
20030927	MM	Added SU1278 tuner.
20030928	MM	Added comments to non-CI (more budget) versions of the card

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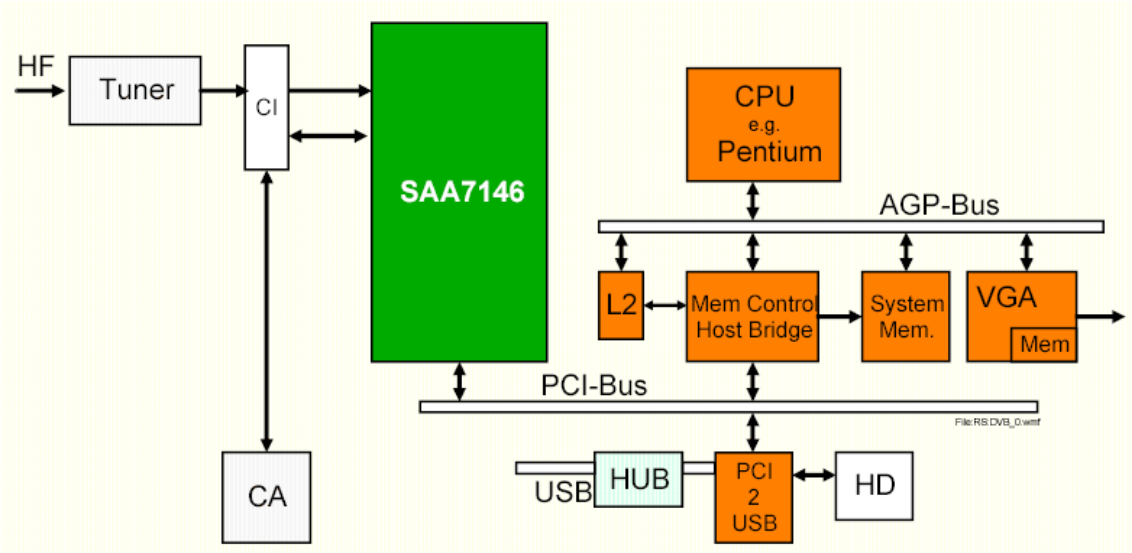
System overview

The following diagram (taken from the Philips reference design 'Sylt') shows an overview of the system:



SDVBACI Rev. 1.0 parts

The TechnoTrend Pcline budget family DVB-S card consist of the following individual parts:

Note: Most of the information also applies to the **B2S1100 Rev. 1.0** cards, which do not have a Common Interface (it is optionally), do not have infrared control (it is optionally) and use a different tuner (Philips SU1278/SH). Note that the B2S1100 Rev. 1.0 card has different designations for components and that some components are different from those on the SDVBACI Rev. 1.0 cards.

SDVBACI Rev. 1.0 Italic designations refer to the B2S1100 Rev. 1.0 cards.			
Reference	Identifier	Manufacturer	Description
U1	-		
U2	-		
U3	N.F.		
U4	-		
U5 *(U12)*	SAA7146A	Philips	Multimedia bridge, high performance scaler and PCI circuit
U6 *(U13)*	24C16	ST	16 kbit serial I2C bus EEPROM
U7	BSRU6-701A	ALPS	Tuner with QPSK demodulator and FEC for digital satellite direct TV receiving With internally: * Philips TDA8060TS Satellite zero-IF QPSK down converter * Philips TSA5059 2.57 GHz I2C-bus controlled low phase noise frequency synthesizer * ST STV0299B QPSK/BPSK link IC
(U9)	*SU1278/SH*	*Philips*	*For internal parts see BSRU6-701A*
U8 *(U10)*	LNBP16SP	ST	LNBP supply and control voltage regulator (parallel interface)
U9	-		
U10 *(U4)*	74HCT4040	Philips	12 stage binary ripple counter
U11 *(U5)*	74HCT74	Philips	Dual D-type flip-flop with set and reset; positive edge trigger
U12	74HCT00	Philips	Quad 2-input NAND gate
U13 *(N.F.)*	MSP430F1101	Texas Instruments	Mixed signal controller 1 kB + 128 B Flash memory, 128 B RAM
U14 *(N.F.)*	74LVC574A	Philips	Octal D-type flip-flop with 5-volt tolerant input/outputs; positive edge trigger (3-state)

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	D1_A0	I/O	MPEG data out 0 (J1)	13	J1
2	D1_A1	I/O	MPEG data out 1 (J1)	14	J1
3	D1_A2	I/O	MPEG data out 2 (J1)	15	J1
4	D1_A3	I/O	MPEG data out 3 (J1)	16	J1
5	VDDD1	P	digital supply voltage 1 (3.3 V)	+3.3V	PCI bus
6	VSSD1	P	digital ground 1	GND	PCI bus
7	D1_A4	I/O	MPEG data out 4 (J1)	17	J1
8	D1_A5	I/O	MPEG data out 5 (J1)	18	J1
9	D1_A6	I/O	MPEG data out 6 (J1)	19	J1
10	D1_A7	I/O	MPEG data out 7 (J1)	20	J1
11	VS_A	I/O	count for MPEG in - start or MPEG out - start 1/512 rate	5	74HCT74
				158	SAA7146A
12	HS_A	I/O	MPEG out - start (J1)	5	74HCT00
				21	J1
13	LLC_A	I/O	MPEG out - clock (J1)	22	J1
14	PXQ_A	I/O	MPEG out - valid (J1)	23	J1
15	VDDD2	P	digital supply voltage 2 (3.3 V)	+3.3V	PCI bus
16	VSSD2	P	digital ground 2	GND	PCI bus
17	TRST	I	test reset input (JTAG pin must be set LOW for normal operation)		
18	TMS	I	test mode select input (JTAG pin must be floating or set to HIGH during normal operation)		
19	TCLK	I	test clock input (JTAG pin should be set LOW during normal operation)		
20	TDO	O	test data output (JTAG pin not active during normal operation)		

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
21	TDI	I	test data input (JTAG pin must be floating or set to HIGH during normal operation)		
22	VDDD3	P	digital supply voltage 3 (3.3 V)	+3.3V	PCI bus
23	VSSD3	P	digital ground 3	GND	PCI bus
24	INTA#	O	PCI interrupt line output (active LOW)	A6	PCI bus
25	RST	I	PCI global reset input (active LOW)	A15	PCI bus
26	CLK	I	PCI clock input	B16	PCI bus
27	GNT#	I	bus grant input signal, PCI arbitration signal (active LOW)	A17	PCI bus
28	REQ#	O	bus request output signal, PCI arbitration signal (active LOW)	B18	PCI bus
29	VDDD4	P	digital supply voltage 4 (3.3 V)	+3.3V	PCI bus
30	VSSD4	P	digital ground 4	GND	PCI bus
31	AD PCI31	I/O	bidirectional PCI multiplexed address/data bit 31	B20	PCI bus
32	AD PCI30	I/O	bidirectional PCI multiplexed address/data bit 30	A20	PCI bus
33	AD PCI29	I/O	bidirectional PCI multiplexed address/data bit 29	B21	PCI bus
34	AD PCI28	I/O	bidirectional PCI multiplexed address/data bit 28	A22	PCI bus
35	VDDD5	P	digital supply voltage 5 (3.3 V)	+3.3V	PCI bus
36	VSSD5	P	digital ground 5	GND	PCI bus
37	AD PCI27	I/O	bidirectional PCI multiplexed address/data bit 27	B23	PCI bus
38	AD PCI26	I/O	bidirectional PCI multiplexed address/data bit 26	A23	PCI bus
39	AD PCI25	I/O	bidirectional PCI multiplexed address/data bit 25	B24	PCI bus
40	AD PCI24	I/O	bidirectional PCI multiplexed address/data bit 24	A25	PCI bus

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
41	C/BE# [3]	I/O	bidirectional PCI multiplexed bus command and byte enable 3 (active LOW)	B26	PCI bus
42	IDSEL	I	PCI initialization device select signal input	A26	PCI bus
43	AD PCI23	I/O	bidirectional PCI multiplexed address/data bit 23	B27	PCI bus
44	AD PCI22	I/O	bidirectional PCI multiplexed address/data bit 22	A28	PCI bus
45	AD PCI21	I/O	bidirectional PCI multiplexed address/data bit 21	B29	PCI bus
46	AD PCI20	I/O	bidirectional PCI multiplexed address/data bit 20	A29	PCI bus
47	VDDD6	P	digital supply voltage 6 (3.3 V)	+3.3V	PCI bus
48	VSSD6	P	digital ground 6	GND	PCI bus
49	AD PCI19	I/O	bidirectional PCI multiplexed address/data bit 19	B30	PCI bus
50	AD PCI18	I/O	bidirectional PCI multiplexed address/data bit 18	A31	PCI bus
51	AD PCI17	I/O	bidirectional PCI multiplexed address/data bit 17	B32	PCI bus
52	AD PCI16	I/O	bidirectional PCI multiplexed address/data bit 16	A32	PCI bus
53	VDDD7	P	digital supply voltage 7 (3.3 V)	+3.3V	PCI bus
54	VSSD7	P	digital ground 7	GND	PCI bus
55	C/BE# [2]	I/O	bidirectional PCI multiplexed bus command and byte enable 2 (active LOW)	B33	PCI bus
56	FRAME#	I/O	bidirectional PCI cycle frame signal (active LOW)	A34	PCI bus
57	IRDY#	I/O	bidirectional PCI initiator ready signal (active LOW)	B35	PCI bus
58	TRDY#	I/O	bidirectional PCI target ready signal (active LOW)	A36	PCI bus
59	DEVSEL#	I/O	bidirectional PCI device select signal (active LOW)	B37	PCI bus
60	STOP#	I/O	bidirectional PCI stop signal (active LOW)	A38	PCI bus

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
61	PERR#	O	PCI parity error signal output (active LOW)	B40	PCI bus
62	PAR	I/O	bidirectional PCI parity signal	A33	PCI bus
63	C/BE# [1]	I/O	bidirectional PCI-bus command and byte enable 1 (active LOW)	B34	PCI bus
64	VDDD8	P	digital supply voltage 8 (3.3 V)	+3.3V	PCI bus
65	VSSD8	P	digital ground 8	GND	PCI bus
66	AD PCI15	I/O	bidirectional PCI multiplexed address/data bit 15	A44	PCI bus
67	AD PCI14	I/O	bidirectional PCI multiplexed address/data bit 14	B45	PCI bus
68	AD PCI13	I/O	bidirectional PCI multiplexed address/data bit 13	A46	PCI bus
69	AD PCI12	I/O	bidirectional PCI multiplexed address/data bit 12	B47	PCI bus
70	VDDD9	P	digital supply voltage 9 (3.3 V)	+3.3V	PCI bus
71	VSSD9	P	digital ground 9	GND	PCI bus
72	AD PCI11	I/O	bidirectional PCI multiplexed address/data bit 11	A47	PCI bus
73	AD PCI10	I/O	bidirectional PCI multiplexed address/data bit 10	B48	PCI bus
74	AD PCI9	I/O	bidirectional PCI multiplexed address/data bit 9	A49	PCI bus
75	AD PCI8	I/O	bidirectional PCI multiplexed address/data bit 8	B52	PCI bus
76	VDDD10	P	digital supply voltage 10 (3.3 V)	+3.3V	PCI bus
77	VSSD10	P	digital ground 10	GND	PCI bus
78	C/BE# [0]	I/O	bidirectional PCI multiplexed bus command and byte enable 0 (active LOW)	A52	PCI bus
79	AD PCI7	I/O	bidirectional PCI multiplexed address/data bit 7	B53	PCI bus
80	AD PCI6	I/O	bidirectional PCI multiplexed address/data bit 6	A54	PCI bus

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
81	VSSD11	P	digital ground 11	GND	PCI bus
82	AD PCI5	I/O	bidirectional PCI multiplexed address/data bit 5	B55	PCI bus
83	AD PCI4	I/O	bidirectional PCI multiplexed address/data bit 4	A55	PCI bus
84	AD PCI3	I/O	bidirectional PCI multiplexed address/data bit 3	B56	PCI bus
85	AD PCI2	I/O	bidirectional PCI multiplexed address/data bit 2	A57	PCI bus
86	VDDD11	P	digital supply voltage 11 (3.3 V)	+3.3V	PCI bus
87	VSSD12	P	digital ground 12	GND	PCI bus
88	AD PCI1	I/O	bidirectional PCI multiplexed address/data bit 1	B58	PCI bus
89	AD PCI0	I/O	bidirectional PCI multiplexed address/data bit 0	A58	PCI bus
90	VDDD12	P	digital supply voltage 12 (3.3 V)	+3.3V	PCI bus
91	VSSD13	P	digital ground 13	GND	PCI bus
92	AD15	I/O	address/data bit 15 (J1) infrared data D7'	48	J1 via 100E
				19	74LVC574
93	AD14	I/O	address/data bit 14 (J1) infrared data D6'	47	J1 via 100E
				18	74LVC574
94	AD13	I/O	address/data bit 13 (J1) infrared data D5'	46	J1 via 100E
				17	74LVC574
95	AD12	I/O	address/data bit 12 (J1) infrared data D4'	45	J1 via 100E
				16	74LVC574
96	VDDD13	P	digital supply voltage 13 (3.3 V)	+3.3V	PCI bus
97	VSSD14	P	digital ground 14	GND	PCI bus
98	AD11	I/O	address/data bit 11 (J1) infrared data D3'	44	J1 via 100E
				15	74LVC574
99	AD10	I/O	address/data bit 10 (J1) infrared data D2'	43	J1 via 100E
				14	74LVC574
100	AD9	I/O	address/data bit 9 (J1) infrared data D1'	42	J1 via 100E
				13	74LVC574

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
101	AD8	I/O	address/data bit 8 (J1) infrared data DO'	41	J1 via 100E
				12	74LVC574
102	VDDD14	P	digital supply voltage 14 (3.3 V)	+3.3V	PCI bus
103	VSSD15	P	digital ground 15	GND	PCI bus
104	RWN_SBHE	O	DEBI data transfer control signal output (read write not/system byte high enable)		
105	AS_ALE	O	latch address	40	J1 via 100E
106	LDS_RDN	O	read# read DEBI	39	J1 via 100E
				1	74LVC574
				11	MSP430F1101
107	UDS_WRN	O	write#	38	J1 via 100E
108	DTACK_RDY	I	extend bus cycle#/transfer ready	37	J1
109	VDDD15	P	digital supply voltage 15 (3.3 V)	+3.3V	PCI bus
110	VSSD16	P	digital ground 16	GND	PCI bus
111	AD0	I/O	address/data bit 0 (J1)	36	J1 via 100E
112	AD1	I/O	address/data bit 1 (J1)	35	J1 via 100E
113	AD2	I/O	address/data bit 2 (J1)	34	J1 via 100E
114	AD3	I/O	address/data bit 3 (J1)	33	J1 via 100E
115	VDDD16	P	digital supply voltage 16 (3.3 V)	+3.3V	PCI bus
116	VSSD17	P	digital ground 17	GND	PCI bus
117	AD4	I/O	address/data bit 4 (J1)	32	J1 via 100E
118	AD5	I/O	address/data bit 5 (J1)	31	J1 via 100E
119	AD6	I/O	address/data bit 6 (J1)	30	J1 via 100E
120	AD7	I/O	address/data bit 7 (J1)	29	J1 via 100E

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
121	WS0	I/O	bidirectional word select signal for audio interface A1		
122	SD0	I/O	bidirectional serial data for audio interface A1		
123	BCLK1	I/O	bidirectional bit clock for audio interface A1		
124	WS1	O	word select output signal for audio interface A1/A2		
125	SD1	I/O	bidirectional serial data for audio interface A1/A2		
126	WS2	O	word select output signal for audio interface A1/A2		
127	SD2	I/O	bidirectional serial data for audio interface A1/A2		
128	VDDD17	P	digital supply voltage 17 (3.3 V)	+3.3V	PCI bus
129	VSSD18	P	digital ground 18	GND	PCI bus
130	WS3	O	word select output signal for audio interface A1/A2		
131	SD3	I/O	bidirectional serial data for audio interface A1/A2		
132	BCLK2	I/O	bidirectional bit clock for audio interface A2		
133	WS4	I/O	bidirectional word select signal for audio interface A2		
134	SD4	I/O	bidirectional serial data for audio interface A2		
135	ACLK	I	audio reference clock input signal		
136	SCL	I/O	I2C clock	20	BSRU6-701A
				6	24C16
				25	J1
137	SDA	I/O	I2C data	21	BSRU6-701A
				5	24C16
				26	J1
138	VDDD18	P	digital supply voltage 18 (3.3 V)	+3.3V	PCI bus
139	VDDI2C	I	I 2 C-bus voltage sense input		
140	VSSD19	P	digital ground 19	GND	PCI bus

SAA7146A (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
141	GPIO3	I/O	general purpose I/O signal 3 infrared data available	11	74LVC574
				12	MSP430F1101
142	GPIO2	I/O	reset# (J1)	28	J1
				14	BSRU6-701A
143	GPIO1	I/O	count on MPEG in - start/MPEG out - start#	1	74HCT00
				2	74HCT00
				13	74HCT00
144	GPIO0	I/O	Common Interface Interrupt#	27	J1
145	D1_B0	I/O	MPEG data in 0 (J1)	34	BSRU6-701A
				12	J1
146	D1_B1	I/O	MPEG data in 1 (J1)	33	BSRU6-701A
				11	J1
147	D1_B2	I/O	MPEG data in 2 (J1)	32	BSRU6-701A
				10	J1
148	D1_B3	I/O	MPEG data in 3 (J1)	31	BSRU6-701A
				9	J1
149	VDDD19	P	digital supply voltage 19 (3.3 V)	+3.3V	PCI bus
150	VSSD20	P	digital ground 20	GND	PCI bus
151	D1_B4	I/O	MPEG data in 4 (J1)	30	BSRU6-701A
				8	J1
152	D1_B5	I/O	MPEG data in 5 (J1)	29	BSRU6-701A
				7	J1
153	D1_B6	I/O	MPEG data in 6 (J1)	28	BSRU6-701A
				6	J1
154	D1_B7	I/O	MPEG data in 7 (J1)	27	BSRU6-701A
				5	J1
155	VDDD20	P	digital supply voltage 20 (3.3 V)	+3.3V	PCI bus
156	VSSD21	P	digital ground 21	GND	PCI bus
157	LLC_B	I/O	MPEG in - clock (J1)	3	J1
				35	BSRU6-701A
158	VS _B	I/O	count for MPEG in - start or MPEG out - start 1/512 rate	5	74HCT74
				11	SAA7146A
159	HS_B	I/O	MPEG in - start (J1)	2	J1
				24	BSRU6-701A
				12	74HCT00
160	PXQ_B	I/O	MPEG in - valid (J1)	26	BSRU6-701A
				1	J1

24C16 (U6)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	E0	I	chip enable 0	GND	PCI bus
2	E1	I	chip enable 1	GND	PCI bus
3	E2	I	chip enable 2	GND	PCI bus
4	VSS	P	ground	GND	PCI bus
5	SDA	I/O	I2C data	137	SAA7146A
				21	BSRU6-701A
				26	J1
6	SCL	I	I2C clock	136	SAA7146A
				20	BSRU6-701A
				25	J1
7	WC#	I	write control	GND	PCI bus
8	VSS	P	supply voltage		PCI bus

BSRU6-701A (U7)							
Source				Internally		Target	
Pin	Symbol	I/O	Description	Pin	Designation	Pin	Designation
1	PWR RF IN	P	power supply input for LNB (RF input)			3	LNBP16SP via diode
2	PWR RF OUT	P	power supply input for LNB (loop out)			-	
3	GND	P	ground			GND	PCI bus
4	+5V 1ST RF	P	power supply input for first RF amplifier				SPS circuitry
						6	BSRU6-701A
						13	BSRU6-701A
						2	BU1 via 56E
5	NC		No connection				
6	+5V SYNTH	P	power supply input IQ demodulator and PLL IC				SPS circuitry
						4	BSRU6-701A
						13	BSRU6-701A
						2	BU1 via 56E
7	DNC		Do not connect			-	
8	DNC		Do not connect			-	
9	NC		No connection			GND	PCI bus
10	GND	P	ground			GND	PCI bus
11	+30V	P	tuning voltage input				circuitry
12	GND	P	ground			GND	PCI bus
13	+5V OTHER	P	power supply input				PSU circuitry
						4	BSRU6-701A
						6	BSRU6-701A
						2	BU1 via 56E
14	RESET#	I	reset# (J1)	15	STV0299B	142	SAA7146A
						28	J1
15	NC		No connection			-	
16	OP0	O	LNB 13V/18V	17	STV0299B	4	LNBP16SP
17	OP1	O	LNB on	18	STV0299B	5	LNBP16SP
18	F22/DiSEqC	O	DiSEqC modulation / 22 kHz tone / programmable output port	16	STV0299B	6	LNBP16SP via coupler

BSRU6-701A (U7)							
Source				Internally		Target	
Pin	Symbol	I/O	Description	Pin	Designation	Pin	Designation
19	LOCK/OP2	O	carrier found / data found / output port 2	19	STV0299B		
20	SCL	I	I2C clock	14	STV0299B	136	SAA7146A
						6	24C16
						25	J1
21	SDA	I/O	I2C data	12	STV0299B	137	SAA7146A
						5	24C16
						26	J1
22	+3.3V	P	+3.3V supply input for QPSK demodulator	13 25	STV0299B		separate regulator
						23	BSRU6-701A via zener
23	+2.5V	P	+2.5V supply input for QPSK demodulator	7 10 30 41 63	STV0299B	22	BSRU6-701A via zener
24	STR_OUT	O	MPEG in - start (J1)	22	STV0299B	12	74HCT00
						2	J1
						159	SAA7146A
25	ERROR	O	error signal output (uncorrectable packet)	20	STV0299B		
26	D/P#	O	MPEG in - valid (J1)	21	STV0299B	160	SAA7146A
						1	J1
27	D[7]/DATA_OUT	O	MPEG data in 7 (J1)	26	STV0299B	154	SAA7146A
						5	J1
28	D[6]	O	MPEG data in 6 (J1)	28	STV0299B	153	SAA7146A
						6	J1
29	D[5]	O	MPEG data in 5 (J1)	29	STV0299B	152	SAA7146A
						7	J1
30	D[4]	O	MPEG data in 4 (J1)	31	STV0299B	151	SAA7146A
						8	J1
31	D[3]	O	MPEG data in 3 (J1)	33	STV0299B	148	SAA7146A
						9	J1
32	D[2]	O	MPEG data in 2 (J1)	34	STV0299B	147	SAA7146A
						10	J1
33	D[1]	O	MPEG data in 1 (J1)	35	STV0299B	146	SAA7146A
						11	J1
34	D[0]	O	MPEG data in 0 (J1)	36	STV0299B	145	SAA7146A
						12	J1
35	CLK_OUT	O	MPEG in - clock (J1)	24	STV0299B	3	J1
						157	SAA7146A

SU1278 (U9) *Note: Informative only, connections have been deduced*							
Source				Internally		Target	
Pin	Symbol	I/O	Description	Pin	Designation	Pin	Designation
1	LNB A	P	power supply input for LNB (RF input)			3	LNBP16SP via diode
2	LNB B	P	power supply input for LNB (loop out)			-	
3	+5V_ENL	P	power supply input for loop-through amplifier				SPS circuitry
						4	SU1278
						2	BU1 via 56E
4	+5V	P	power supply input IQ demodulator and PLL IC				SPS circuitry
						3	SU1278
						2	BU1 via 56E
5	+2.5V	P	+2.5V supply input for QPSK demodulator	7 10 30 41 63	STV0299B		
6	Vt	P	Tuning supply voltage +30V				circuitry
7	AS	I	Address select of tuner synthesizer			GND	PCI bus
8	IP0	I	Input port				
9	D[0]	O	MPEG data in 0 (J1)	36	STV0299B	145	SAA7146A
						12	J1
10	D[1]	O	MPEG data in 1 (J1)	35	STV0299B	146	SAA7146A
						11	J1
11	D[2]	O	MPEG data in 2 (J1)	34	STV0299B	147	SAA7146A
						10	J1
12	D[3]	O	MPEG data in 3 (J1)	33	STV0299B	148	SAA7146A
						9	J1
13	D[4]	O	MPEG data in 4 (J1)	31	STV0299B	151	SAA7146A
						8	J1
14	D[5]	O	MPEG data in 5 (J1)	29	STV0299B	152	SAA7146A
						7	J1
15	D[6]	O	MPEG data in 6 (J1)	28	STV0299B	153	SAA7146A
						6	J1
16	D[7]/DATA_OUT	O	MPEG data in 7 (J1)	26	STV0299B	154	SAA7146A
						5	J1

SU1278 (U9) *Note: Informative only, connections have been deduced*							
Source				Internally		Target	
Pin	Symbol	I/O	Description	Pin	Designation	Pin	Designation
17	CLK_OUT	O	MPEG in - clock (J1)	24	STV0299B	3	J1
						157	SAA7146A
18	STR_OUT	O	MPEG in - start (J1)	22	STV0299B	12	74HCT00
						2	J1
						159	SAA7146A
19	D/P#	O	MPEG in - valid (J1)	21	STV0299B	160	SAA7146A
						1	J1
20	ERROR	O	error signal output (uncorrectable packet)	20	STV0299B		
21	GND	P	ground			GND	PCI bus
22	LOCK/OP2	O	carrier found / data found / output port 2	19	STV0299B		
23	OP1	O	LNB on	18	STV0299B	5	LNBP16SP
24	OP0	O	LNB 13V/18V	17	STV0299B	4	LNBP16SP
25	F22/DiSEqC	O	DiSEqC modulation / 22 kHz tone / programmable output port	16	STV0299B	6	LNBP16SP via coupler
26	RESET#	I	reset# (J1)	15	STV0299B	142	SAA7146A
						28	J1
27	SCL	I	I2C clock	14	STV0299B	136	SAA7146A
						6	24C16
						25	J1
28	SDA	I/O	I2C data	12	STV0299B	137	SAA7146A
						5	24C16
						26	J1

LNBP16SP (U8)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	VCC1	P	supply input 1	+++	generated V+
				2	LNBP16SP
2	VCC2	P	supply input 2	+++	generated V+
				1	LNBP16SP
3	LNBA	O	output port	1	BSRU6-701A via diode
4	VSEL	I	LNB 13V/18V	16	BSRU6-701A
5	EN	I	LNB on	17	BSRU6-701A
6	GND	P	ground	GND	PCI bus
7	ENT	I	22 kHz tone enable	GND	PCI bus
8	CEXT	I	external capacitor		capacitor
9	EXTM	I	external modulation input	18	BSRU6-701A via coupler
10	LLC	I	line length compensation	-	

74HCT4040 (U10)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	Q11	O	parallel output 11 1/2048	-	
2	Q5	O	parallel output 5 1/32	-	
3	Q4	O	parallel output 4 1/16	-	
4	Q6	O	parallel output 6 1/64	-	
5	Q3	O	parallel output 3 1/8	-	
6	Q2	O	parallel output 2 1/4	-	
7	Q1	O	parallel output 1 1/2	-	
8	GND	P	ground	GND	PCI bus
9	Q0	O	parallel output 0 1/1	-	
10	CP#	I	count for MPEG in - start or MPEG out - start	8	74HCT00
				3	74HCT74
11	MR	I	master reset input (active high)	GND	PCI bus
12	Q8	O	parallel output 8 can be linked via R39 (not fitted) 1/256	2	74HCT74 via R39, R40, R41
13	Q7	O	parallel output 7 1/128	-	
14	Q9	O	parallel output 9 can be linked via R40 (OE) **** Q9 selected as output 1/512	2	74HCT74 via R39, R40, R41
15	Q10	O	parallel output 10 can be linked via R41 (not fitted) 1/1024	2	74HCT74 via R39, R40, R41
16	VCC	P	positive supply voltage	+5V	PCI bus

74HCT74 (U11)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	1R#	I		+5V	PCI bus
2	1D	I	count for MPEG in - start or MPEG out - start 1/x rate	14	74HCT4040 via R40 (OE)
3	1CP	I	count for MPEG in - start or MPEG out - start	8	74HCT00
				10	74HCT4040
4	1S#	I		+5V	PCI bus
5	1Q	O	count for MPEG in - start or MPEG out - start 1/512 rate	11 158	SAA7146A
6	1Q#	O		-	
7	GND	P	ground	GND	PCI bus
8	2Q#	O		-	
9	2Q	O		-	
10	2S#	I		+5V	PCI bus
11	2CP	I		+5V	PCI bus
12	2D	I		+5V	PCI bus
13	2R#	I		+5V	PCI bus
14	VCC	P	positive power supply	+5V	PCI bus

74HCT00 (U12)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	1A	I	count on MPEG in - start/MPEG out - start#	143	SAA7146A
				2	74HCT00
				13	74HCT00
2	1B	I	count on MPEG in - start/MPEG out - start#	143	SAA7146A
				1	74HCT00
				13	74HCT00
3	1Y	O	count on MPEG in - start#/MPEG out - start	4	74HCT00
4	2A	I	count on MPEG in - start#/MPEG out - start	3	74HCT00
5	2B	I	MPEG out - start (J1)	12	SAA7146A
				21	J1
6	2Y	O	count for MPEG out - start	9	74HCT00
7	GND	P	ground	GND	PCI bus
8	3Y	O	count for MPEG in - start or MPEG out - start	3	74HCT74
				10	74HCT4040
9	3A	I	count for MPEG out - start	6	74HCT00
10	3B	I	count for MPEG in - start	11	74HCT00
11	4Y	O	count for MPEG in - start	10	74HCT00
12	4A	I	MPEG in - start (J1)	24	BRSU6-701A
				2	J1
				159	SAA7146A
13	4B	I	count on MPEG in - start/MPEG out - start#	143	SAA7146A
				1	74HCT00
				2	74HCT00
14	VCC	P	positive power supply	+5V	PCI bus

MSP430F1101 (U13)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	TEST	I	select of test mode for JTAG pins on port 1	4	J3
2	VCC	P	supply voltage	+3.3V	PCI bus
3	P2.5	I/O	general purpose digital I/O pin		
4	VSS	P	ground	GND	PCI bus
5	XOUT	I/O	output terminal of crystal oscillator		
6	XIN	I	input terminal of crystal oscillator		
7	RST#/NMI	I	reset or non maskable interrupt input	2	J3
8	P2.0	I/O	general purpose digital I/O pin		
9	P2.1	I/O	general purpose digital I/O pin	10	MSP430F1101
				3	BU1 via transistor
10	P2.2	I/O	general purpose digital I/O pin	9	MSP430F1101
				3	BU1 via transistor
11	P2.3	I/O	general purpose digital I/O pin	1	74LVC574
				106	SAA7146A
				39	J1 via 100E
12	P2.4	I/O	general purpose digital I/O pin infrared data available	11	74LVC574
13	P1.0	I/O	general purpose digital I/O pin infrared data D0	9	74LVC574
14	P1.1	I/O	general purpose digital I/O pin infrared data D1	8	74LVC574
15	P1.2	I/O	general purpose digital I/O pin infrared data D2	7	74LVC574
16	P1.3	I/O	general purpose digital I/O pin infrared data D3	6	74LVC574
17	P1.4	I/O	general purpose digital I/O pin infrared data D4	5	74LVC574
18	P1.5	I/O	general purpose digital I/O pin infrared data D5	4	74LVC574
19	P1.6	I/O	general purpose digital I/O pin infrared data D6	3	74LVC574
20	P1.7	I/O	general purpose digital I/O pin infrared data D7	2	74LVC574

74LVC574 (U14)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	OE#	I	output enable input (active low) read DEBI	106	SAA7146A
				11	MSP430F1101
				39	J1 via 100E
2	D0	I	data input 0 infrared data D7	20	MSP430F1101
3	D1	I	data input 1 infrared data D6	19	MSP430F1101
4	D2	I	data input 2 infrared data D5	18	MSP430F1101
5	D3	I	data input 3 infrared data D4	17	MSP430F1101
6	D4	I	data input 4 infrared data D3	16	MSP430F1101
7	D5	I	data input 5 infrared data D2	15	MSP430F1101
8	D6	I	data input 6 infrared data D1	14	MSP430F1101
9	D7	I	data input 7 infrared data D0	13	MSP430F1101
10	GND	P	ground	GND	PCI bus

74LVC574 (U14)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
11	CP	I	clock input (low to high, edge triggered) infrared data available	12	MSP430F1101
				141	SAA7146A
12	Q7	O	address bit 8 (J1) infrared data D0'	101	SAA7146A
				41	J1 via 100E
13	Q6	O	address bit 9 (J1) infrared data D1'	100	SAA7146A
				42	J1 via 100E
14	Q5	O	address bit 10 (J1) infrared data D2'	99	SAA7146A
				43	J1 via 100E
15	Q4	O	address bit 11 (J1) infrared data D3'	98	SAA7146A
				44	J1 via 100E
16	Q3	O	address bit 12 (J1) infrared data D4'	95	SAA7146A
				45	J1 via 100E
17	Q2	O	address bit 13 (J1) infrared data D5'	94	SAA7146A
				46	J1 via 100E
18	Q1	O	address bit 14 (J1) infrared data D6'	93	SAA7146A
				47	J1 via 100E
19	Q0	O	address bit 15 (J1) infrared data D7'	92	SAA7146A
				48	J1 via 100E
20	VCC	P	positive power supply	+3.3V	PCI bus

COMMON INTERFACE (J1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1			MPEG in - valid (J1)	160	SAA7146A
				26	BSRU6-701A
2			MPEG in - start (J1)	159	SAA7146A
				24	BSRU6-701A
				12	74HCT00
3			MPEG in - clock (J1)	157	SAA7146A
				35	BSRU6-701A
4	GND		ground	GND	PCI bus
5			MPEG data in 7 (J1)	154	SAA7146A
				27	BSRU6-701A
6			MPEG data in 6 (J1)	153	SAA7146A
				28	BSRU6-701A
7			MPEG data in 5 (J1)	152	SAA7146A
				29	BSRU6-701A
8			MPEG data in 4 (J1)	151	SAA7146A
				30	BSRU6-701A
9			MPEG data in 3 (J1)	148	SAA7146A
				31	BSRU6-701A
10			MPEG data in 2 (J1)	147	SAA7146A
				32	BSRU6-701A
11			MPEG data in 1 (J1)	146	SAA7146A
				33	BSRU6-701A
12			MPEG data in 0 (J1)	145	SAA7146A
				34	BSRU6-701A
13			MPEG data out 0 (J1)	1	SAA7146A
14			MPEG data out 1 (J1)	2	SAA7146A
15			MPEG data out 2 (J1)	3	SAA7146A
16			MPEG data out 3 (J1)	4	SAA7146A
17			MPEG data out 4 (J1)	7	SAA7146A
18			MPEG data out 5 (J1)	8	SAA7146A
19			MPEG data out 6 (J1)	9	SAA7146A
20			MPEG data out 7 (J1)	10	SAA7146A

COMMON INTERFACE (J1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
21			MPEG out - start (J1)	12	SAA7146A
				5	74HCT00
22			MPEG out - clock (J1)	13	SAA7146A
23			MPEG out - valid (J1)	14	SAA7146A
24	GND		ground	GND	PCI bus
25			I2C clock	136	SAA7146A
				6	24C16
				20	BSRU6-701A
26			I2C data	137	SAA7146A
				5	24C16
				21	BSRU6-701A
27			Common Interface Interrupt#	144	SAA7146A
28			reset (J1)	142	SAA7146A
				14	BSRU6-701A
29			address bit 7 (J1)	120	SAA7146A via 100E
30			address bit 6 (J1)	119	SAA7146A via 100E
31			address bit 5 (J1)	118	SAA7146A via 100E
32			address bit 4 (J1)	117	SAA7146A via 100E
33			address bit 3 (J1)	114	SAA7146A via 100E
34			address bit 2 (J1)	113	SAA7146A via 100E
35			address bit 1 (J1)	112	SAA7146A via 100E
36			address bit 0 (J1)	111	SAA7146A via 100E
37		I	extend bus cycle#/transfer ready	108	SAA7146A
38			write#	107	SAA7146A via 100E
39			read#	106	SAA7146A via 100E
				11	MSP430F1101
				1	74LVC574
40			latch address	105	SAA7146A via 100E

COMMON INTERFACE (J1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
41			address bit 8 (J1)	101	SAA7146A via 100E
				12	74LVC574 via 100E
42			address bit 9 (J1)	100	SAA7146A via 100E
				13	74LVC574 via 100E
43			address bit 10 (J1)	99	SAA7146A via 100E
				14	74LVC574 via 100E
44			address bit 11 (J1)	98	SAA7146A via 100E
				15	74LVC574 via 100E
45			address bit 12 (J1)	95	SAA7146A via 100E
				16	74LVC574 via 100E
46			address bit 13 (J1)	94	SAA7146A via 100E
				17	74LVC574 via 100E
47			address bit 14 (J1)	93	SAA7146A via 100E
				18	74LVC574 via 100E
48			address bit 15 (J1)	92	SAA7146A via 100E
				19	74LVC574 via 100E
49	+5V		positive power supply	+5V	PCI bus
50	+5V		positive power supply	+5V	PCI bus

JTAG MSP430F1101 (J3)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1					
2			reset	7	MSP430F1101
3					
4			JTAG	1	MSP430F1101
5					
6			power supply	+3.3V	PCI bus
7					
8			ground	GND	PCI bus

INFRARED (BU1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	GND	P	ground	GND	PCI bus
2	V+	P	positive power supply	6	BSRU6-701A via 56E
3	INFRARED	I	infrared input	9 10	MDP430F1101 via transistor

BDGTCIS Rev. 1.0 parts

The TechnoTrend Pcline budget family common interface card consist of the following individual parts:

BDGTCIS Rev. 1.0			
Reference	Identifier	Manufacturer	Description
U1	LD33C	ST	Regulator 3.3V (?)
U2	M4A3-32-10VC-12	Lattice	ispMach high performance E2CMOS in system programmable logic
U3	74LVC573A	Philips	Octal D-type transparent latch with 5-volt tolerant input/outputs (3-state)
U4	74LVC573A	Philips	Octal D-type transparent latch with 5-volt tolerant input/outputs (3-state)
U5	74LVC573A	Philips	Octal D-type transparent latch with 5-volt tolerant input/outputs (3-state)
U6	74LVC244A	Philips	Octal buffer / line driver; 3-state
U7	74LVC573A	Philips	Octal D-type transparent latch with 5-volt tolerant input/outputs (3-state)
U8	74LVC00A	Philips	Quad 2-input NAND gate

M4A3-32 (U2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	I/O 5	I/O	address bit 5 (J1)	29	J1 with 10k pull down
				9	U3-74LVC573
2	I/O 6	I/O	address bit 6 (J1)	30	J1 with 10k pull down
				8	U3-74LVC573
3	I/O 7	I/O	address bit 7 (J1)	31	J1 with 10k pull down
				7	U3-74LVC573
4	TDI	I	test data in		
5	CLKO/10	I	reset# (J1)	28	J1
6	NC				
7	GND	P	ground	GND	
8	TCK	I	test clock		
9	I/O 8	I/O	Common Interface Interrupt#	27	J1
10	I/O 9	I/O	register select#	61	J2
11	I/O 10	I/O	I/O read#	44	J2
12	I/O 11	I/O	I/O write#	45	J2
13	I/O 12	I/O	enable MPEG data to/from CI#	1	U5-74LVC573
				1	U6-74LVC244
				19	U6-74LVC244
				1	U7-74LVC573
14	I/O 13	I/O	card enable 1#	7	J2
15	I/O 14	I/O	write enable#	15	J2
16	I/O 15	I/O	output enable#	9	J2
17	VCC	P	positive power supply	-	
18	NC				
19	GND	P	ground		
20	I/O 16	I/O	data bit 7 (CI)	6	J2

M4A3-32 (U2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
21	I/O 17	I/O	data bit 6 (CI)	5	J2
22	I/O 18	I/O	data bit 5 (CI)	4	J2
23	I/O 19	I/O	data bit 4 (CI)	3	J2
24	I/O 20	I/O	data bit 3 (CI)	2	J2
25	I/O 21	I/O	data bit 2 (CI)	32	J2
26	I/O 22	I/O	data bit 1 (CI)	31	J2
27	I/O 23	I/O	data bit 0 (CI)	30	J2
28	TMS	I	test mode select		
29	CLK1/I1	I	interrupt request	16	J2
30	NC				
31	GND	P	ground	GND	
32	TDO	O	test data out		
33	I/O 24	I/O	card reset	58	J2
34	I/O 25	I/O	address bit 12 (J1)	45	J1 with 10k pull down
				6	U4-74LVC573
35	I/O 26	I/O	address bit 13 (J1)	46	J1 with 10k pull down
				7	U4-74LVC573
36	I/O 27	I/O	address bit 14 (J1)	47	J1 with 10k pull down
				8	U4-74LVC573
37	I/O 28	I/O	latch address	40	J1
				11	U3-74LVC573
				11	U4-74LVC573
38	I/O 29	I/O	card detect#	8	U8-74LVC00
				1	U3-74LVC573
				1	U4-74LVC573
39	I/O 30	I/O	read#	39	J1
40	I/O 31	I/O	write#	38	J1

M4A3-32 (U2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
41	VCC	P	positive power supply	+3.3V	U1
42	NC				
43	GND	P	ground	GND	
44	I/O 0	I/O	address bit 0 (J1)	36	J1 with 10k pull down
				2	U3-74LVC573
45	I/O 1	I/O	address bit 1 (J1)	35	J1 with 10k pull down
				3	U3-74LVC573
46	I/O 2	I/O	address bit 2 (J1)	34	J1 with 10k pull down
				4	U3-74LVC573
47	I/O 3	I/O	address bit 3 (J1)	33	J1 with 10k pull down
				5	U3-74LVC573
48	I/O 4	I/O	address bit 4 (J1)	32	J1 with 10k pull down
				6	U3-74LVC573

74LVC573 (U3)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	OE#	I	card detect#	38	U2-M4A3-32
				1	U4-74LVC573
				8	U8-74LVC00
2	D0	I	address bit 0 (J1)	36	J1 with 10k pull down
				44	U2-M4A3-32
3	D1	I	address bit 1 (J1)	35	J1 with 10k pull down
				45	U2-M4A3-32
4	D2	I	address bit 2 (J1)	34	J1 with 10k pull down
				46	U2-M4A3-32
5	D3	I	address bit 3 (J1)	33	J1 with 10k pull down
				47	U2-M4A3-32
6	D4	I	address bit 4 (J1)	32	J1 with 10k pull down
				48	U2-M4A3-32
7	D5	I	address bit 5 (J1)	31	J1 with 10k pull down
				3	U2-M4A3-32
8	D6	I	address bit 6 (J1)	30	J1 with 10k pull down
				2	U2-M4A3-32
9	D7	I	address bit 7 (J1)	29	J1 with 10k pull down
				1	U2-M4A3-32
10	GND	P	ground	GND	
11	CP	I	latch address	40	J1
				37	U2-M4A3-32
				11	U4-74LVC573
12	Q7	O	address bit 7 (CI)	22	J2
13	Q6	O	address bit 6 (CI)	23	J2
14	Q5	O	address bit 5 (CI)	24	J2
15	Q4	O	address bit 4 (CI)	25	J2
16	Q3	O	address bit 3 (CI)	26	J2
17	Q2	O	address bit 2 (CI)	27	J2
18	Q1	O	address bit 1 (CI)	28	J2
19	Q0	O	address bit 0 (CI)	29	J2
20	VCC	P	positive power supply	+3.3V	U1

74LVC573 (U4)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	OE#	I	card detect#	38	U2-M4A3-32
				1	U3-74LVC573
				8	U8-74LVC00
2	D0	I	address bit 8 (J1)	41	J1 with 10k pull down
3	D1	I	address bit 9 (J1)	42	J1 with 10k pull down
4	D2	I	address bit 10 (J1)	43	J1 with 10k pull down
5	D3	I	address bit 11 (J1)	44	J1 with 10k pull down
6	D4	I	address bit 12 (J1)	34	U2-M4A3-32
				45	J1 with 10k pull down
7	D5	I	address bit 13 (J1)	35	U2-M4A3-32
				46	J1 with 10k pull down
8	D6	I	address bit 14 (J1)	36	U2-M4A3-32
				47	J1 with 10k pull down
9	D7	I	address bit 15 (J1)	37	U2-M4A3-32
				48	J1 with 10k pull down
10	GND	P	ground	GND	
11	CP	I	latch address	40	J1
				37	U2-M4A3-32
				11	U3-74LVC573
12	Q7	O	address bit 15 (–)		
13	Q6	O	address bit 14 (–)		
14	Q5	O	address bit 13 (–)		
15	Q4	O	address bit 12 (–)		
16	Q3	O	address bit 11 (CI)	10	J2
17	Q2	O	address bit 10 (CI)	8	J2
18	Q1	O	address bit 9 (CI)	11	J2
19	Q0	O	address bit 8 (CI)	12	J2
20	VCC	P	positive power supply	+3.3V	U1

74LVC573 (U5)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	OE#	I	enable data to/from CI#	13	U2-M4A3-32 with 10k pull up
				1	U6-74LVC244
				1	U7-74LVC573
2	D0	I	MPEG data in 0 (J1)	12	J1
3	D1	I	MPEG data in 1 (J1)	11	J1
4	D2	I	MPEG data in 2 (J1)	10	J1
5	D3	I	MPEG data in 3 (J1)	9	J1
6	D4	I	MPEG data in 4 (J1)	8	J1
7	D5	I	MPEG data in 5 (J1)	7	J1
8	D6	I	MPEG data in 6 (J1)	6	J1
9	D7	I	MPEG data in 7 (J1)	5	J1
10	GND	P	ground	GND	
11	CP	I		+3.3V	U1
12	Q7	O	MPEG data in 7 (CI)	56	J2
13	Q6	O	MPEG data in 6 (CI)	55	J2
14	Q5	O	MPEG data in 5 (CI)	54	J2
15	Q4	O	MPEG data in 4 (CI)	53	J2
16	Q3	O	MPEG data in 3 (CI)	50	J2
17	Q2	O	MPEG data in 2 (CI)	49	J2
18	Q1	O	MPEG data in 1 (CI)	48	J2
19	Q0	O	MPEG data in 0 (CI)	47	J2
20	VCC	P	positive power supply	+3.3V	U1

74LVC244 (U6)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	OE1#	I	enable data to/from CI#	19	U6-74LVC244
				13	U2-M4A3-32 with 10k pull up
				1	U5-74LVC573
				1	U7-74LVC573
2	D0	I	MPEG in - start (J1)	2	J1
3	Q1	O	MPEG data out 4 (J1)	17	J1 via 100E
4	D2	I	MPEG in - valid (J1)	1	J1
5	Q3	O	MPEG data out 5 (J1)	18	J1 via 100E
6	D4	I	MPEG in - clock (J1)	3	J1
7	Q5	O	MPEG data out 6 (J1)	19	J1 via 100E
8	D6	I		GND	
9	Q7	O	MPEG data out 7 (J1)	20	J1 via 100E
10	GND	P	ground	GND	
11	D7	I	MPEG data out 7 (CI)	41	J2
12	Q6	O		-	
13	D5	I	MPEG data out 6 (CI)	40	J2
14	Q4	O	MPEG in - clock (CI)	20	J2 via 50E
15	D3	I	MPEG data out 5 (CI)	39	J2
16	Q2	O	MPEG in - valid (CI)	19	J2
17	D1	I	MPEG data out 4 (CI)	38	J2
18	Q0	O	MPEG in - start (CI)	46	J2
19	OE2#	I	enable data to/from CI#	1	U6-74LVC244
				13	U2-M4A3-32 with 10k pull up
				1	U5-74LVC573
				1	U7-74LVC573
20	VCC	P	positive power supply	+3.3V	U1

74LVC573 (U7)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	OE#	I	enable data to/from CI#	13	U2-M4A3-32 with 10k pull up
				1	U5-74LVC573
				1	U6-74LVC244
2	D0	I		GND	
3	D1	I	MPEG out - clock (CI)	57	J2
4	D2	I	MPEG out - valid (CI)	62	J2
5	D3	I	MPEG out - start (CI)	63	J2
6	D4	I	MPEG data out 3 (CI)	37	J2
7	D5	I	MPEG data out 0 (CI)	64	J2
8	D6	I	MPEG data out 1 (CI)	65	J2
9	D7	I	MPEG data out 2 (CI)	66	J2
10	GND	P	ground	GND	
11	CP	I		+3.3V	U1
12	Q7	O	MPEG data out 2 (J1)	15	J1 via 100E
13	Q6	O	MPEG data out 1 (J1)	14	J1 via 100E
14	Q5	O	MPEG data out 0 (J1)	13	J1 via 100E
15	Q4	O	MPEG data out 3 (J1)	16	J1 via 100E
16	Q3	O	MPEG out - start (J1)	21	J1 via 100E
17	Q2	O	MPEG out - valid (J1)	23	J1 via 100E
18	Q1	O	MPEG out - clock (J1)	22	J1 via 100E
19	Q0	O		-	
20	VCC	P	positive power supply	+3.3V	U1

74LVC00 (U8)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	1A	I	card detect 2#	67	J2
				2	U8-74LVC00
2	1B	I	card detect 2#	67	J2
				1	U8-74LVC00
3	1Y	O	card detect 2	9	U8-74LVC00
4	2A	I			
5	2B	I			
6	2Y	O			
7	GND	P	ground	GND	
8	3Y	O	card detect#	38	U2-M4A3-32
				1	U3-74LVC573
				1	U4-74LVC573
9	3A	I	card detect 2	3	U8-74LVC00
10	3B	I	card detect 1	11	74LVC00
11	4Y	O	card detect 1	10	74LVC00
12	4A	I	card detect 1#	36	J2
				13	74LVC00 with 10k pull up
13	4B	I	card detect 1#	36	J2
				12	74LVC00 with 10k pull up
14	VCC	P	positive power supply	+3.3V	U1

COMMON INTERFACE (J1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1			MPEG in - valid (J1)	4	U6-74LVC244
2			MPEG in - start (J1)	2	U6-74LVC244
3			MPEG in - clock (J1)	6	U6-74LVC244
4	GND		ground	GND	
5			MPEG data in 7 (J1)	9	U5-74LVC573
6			MPEG data in 6 (J1)	8	U5-74LVC573
7			MPEG data in 5 (J1)	7	U5-74LVC573
8			MPEG data in 4 (J1)	6	U5-74LVC573
9			MPEG data in 3 (J1)	5	U5-74LVC573
10			MPEG data in 2 (J1)	4	U5-74LVC573
11			MPEG data in 1 (J1)	3	U5-74LVC573
12			MPEG data in 0 (J1)	2	U5-74LVC573
13			MPEG data out 0 (J1)	14	U7-74LVC573 via 100E
14			MPEG data out 1 (J1)	13	U7-74LVC573 via 100E
15			MPEG data out 2 (J1)	12	U7-74LVC573 via 100E
16			MPEG data out 3 (J1)	15	U7-74LVC573 via 100E
17			MPEG data out 4 (J1)	3	U6-74LVC244 via 100E
18			MPEG data out 5 (J1)	5	U6-74LVC244 via 100E
19			MPEG data out 6 (J1)	7	U6-74LVC244 via 100E
20			MPEG data out 7 (J1)	9	U6-74LVC244 via 100E

COMMON INTERFACE (J1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
21			MPEG out - start (J1)	16	U7-74LVC573 via 100E
22			MPEG2 out - clock (J1)	18	U7-74LVC573 via 100E
23			MPEG out - valid (J1)	17	U7-74LVC573 via 100E
24	GND		ground	GND	
25			I2C clock		
26			I2C data		
27			Common Interface Interrupt#	9	U2-M4A3-32
28			reset# (J1)	5	U2-M4A3-32
29			address bit 7 (J1)	9	U3-74LVC573 with 10k pull down
				1	U2-M4A3-32
30			address bit 6 (J1)	8	U3-74LVC573 with 10k pull down
				2	U2-M4A3-32
31			address bit 5 (J1)	7	U3-74LVC573 with 10k pull down
				1	U2-M4A3-32
32			address bit 4 (J1)	6	U3-74LVC573 with 10k pull down
				48	U2-M4A3-32
33			address bit 3 (J1)	5	U3-74LVC573 with 10k pull down
				47	U2-M4A3-32
34			address bit 2 (J1)	4	U3-74LVC573 with 10k pull down
				46	U2-M4A3-32
35			address bit 1 (J1)	3	U3-74LVC573 with 10k pull down
				45	U2-M4A3-32
36			address bit 0 (J1)	2	U3-74LVC573 with 10k pull down
				44	U2-M4A3-32
37		I	extend bus cycle#/transfer ready	59	J2 via 100E
38			write#	40	U2-M4A3-32
39			read#	39	U2-M4A3-32
40			latch address	37	U2-M4A3-32
				11	U3-74LVC573
				11	U4-74LVC573

COMMON INTERFACE (J1)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
41			address bit 8 (J1)	2	U4-74LVC573 with 10k pull down
42			address bit 9 (J1)	3	U4-74LVC573 with 10k pull down
43			address bit 10 (J1)	4	U4-74LVC573 with 10k pull down
44			address bit 11 (J1)	5	U4-74LVC573 with 10k pull down
45			address bit 12 (J1)	34	U2-M4A3-32
				6	U4-74LVC573 with 10k pull down
46			address bit 13 (J1)	35	U2-M4A3-32
				7	U4-74LVC573 with 10k pull down
47			address bit 14 (J1)	36	U2-M4A3-32
				8	U4-74LVC573 with 10k pull down
48			address bit 15 (J1)	9	U4-74LVC573 with 10k pull down
49	VCC	P	positive power supply	+5V	U1
50	VCC	P	positive power supply	+5V	U1

PCMCIA / PC CARD (J2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1	GND	P	ground		
2	D3	I/O	data bit 3 (CI)	24	U2-M4A3-32
3	D4	I/O	data bit 4 (CI)	23	U2-M4A3-32
4	D5	I/O	data bit 5 (CI)	22	U2-M4A3-32
5	D6	I/O	data bit 6 (CI)	21	U2-M4A3-32
6	D7	I/O	data bit 7 (CI)	20	U2-M4A3-32
7	CE1#	I	card enable 1	14	U2-M4A3-32
8	A10	I	address bit 10 (CI)	17	U4-74LVC573
9	OE#	I	output enable	16	U2-M4A3-32
10	A11	I	address bit 11 (CI)	16	U4-74LVC573
11	A9	I	address bit 9 (CI)	18	U4-74LVC573
12	A8	I	address bit 8 (CI)	19	U4-74LVC573
13	A13	I		GND	
14	A14	I		GND	
15	WE#	I	write enable	15	U2-M4A3-32
16	IREQ#	O	interrupt request	29	U2-M4A3-32
17	VCC	P	positive power supply		
18	VPP1	P	program voltage 1		
19	MIVAL	I	MPEG in - valid (CI)	16	U6-74LVC244
20	MCLKI	I	MPEG in - clock (CI)	14	U6-74LVC244

PCMCIA / PC CARD (J2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
21	A12	I		GND	
22	A7	I	address bit 7 (CI)	12	U3-74LVC573
23	A6	I	address bit 6 (CI)	13	U3-74LVC573
24	A5	I	address bit 5 (CI)	14	U3-74LVC573
25	A4	I	address bit 4 (CI)	15	U3-74LVC573
26	A3	I	address bit 3 (CI)	16	U3-74LVC573
27	A2	I	address bit 2 (CI)	17	U3-74LVC573
28	A1	I	address bit 1 (CI)	18	U3-74LVC573
29	A0	I	address bit 0 (CI)	19	U3-74LVC573
30	D0	I/O	data bit 0 (CI)	27	U2-M4A3-32
31	D1	I/O	data bit 1 (CI)	26	U2-M4A3-32
32	D2	I/O	data bit 2 (CI)	25	U2-M4A3-32
33	IOIS16#	O	16 bit I/O (always high)		
34	GND	P	ground		

PCMCIA / PC CARD (J2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
35	GND	P	ground	GND	
36	CD1#	O	card detect 1	12	U8-74LVC00 with 10k pull up
				13	U8-74LVC00 with 10k pull up
37	MDO3	O	MPEG data out 3 (CI)	6	U7-74LVC573
38	MDO4	O	MPEG data out 4 (CI)	17	U6-74LVC244
39	MDO5	O	MPEG data out 5 (CI)	15	U6-74LVC244
40	MDO6	O	MPEG data out 6 (CI)	13	U6-74LVC244
41	MDO7	O	MPEG data out 7 (CI)	11	U6-74LVC244
42	CE2#	I	card enable 2	+3.3V	U1
43	VS1#	O	voltage sense 1		
44	IORD#	I	I/O read	11	U2-M4A3-32
45	IOWR#	I	I/O write	12	U2-M4A3-32
46	MISTRT	I	MPEG in - start (CI)	18	U6-74LVC244
47	MDI0	I	MPEG data in 0 (CI)	19	U5-74LVC573
48	MDI1	I	MPEG data in 1 (CI)	18	U5-74LVC573
49	MDI2	I	MPEG data in 2 (CI)	17	U5-74LVC573
50	MDI3	I	MPEG data in 3 (CI)	16	U5-74LVC573
51	VCC	P	positive power supply	15	U5-74LVC573
52	VPP2	P	program voltage 2		
53	MDI4	I	MPEG data in 4 (CI)	14	U5-74LVC573
54	MDI5	I	MPEG data in 5 (CI)	13	U5-74LVC573

PCMCIA / PC CARD (J2)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
55	MDI6	I	MPEG data in 6 (CI)	12	U5-74LVC573
56	MDI7	I	MPEG data in 7 (CI)	11	U5-74LVC573
57	MCLKO	O	MPEG out - clock (CI)	3	U7-74LVC573
58	RESET	I	card reset	33	U2-M4A3-32
59	WAIT#	O	extend bus cycle#/transfer ready	37	J1 via 100E
60	INPACK#	O	input port acknowledge		
61	REG#	I	register select	10	U2-M4A3-32
62	MOVAL	O	MPEG out - valid (CI)	4	U7-74LVC573
63	MOSTRT	O	MPEG out - start (CI)	5	U7-74LVC573
64	MDO0	O	MPEG data out 0 (CI)	7	U7-74LVC573
65	MDO1	O	MPEG data out 1 (CI)	8	U7-74LVC573
66	MDO2	O	MPEG data out 2 (CI)	9	U7-74LVC573
67	CD2#	O	card detect 2	1	U8-74LVC00
				2	U8-74LVC00
68	GND	P	ground	GND	

JTAG M4A3-32 (J3)					
Source				Target	
Pin	Symbol	I/O	Description	Pin	Designation
1					
2			reset		
3					
4			JTAG		
5					
6			power supply	+3.3V	
7					
8			ground	GND	PCI bus

Hardware I/O list

The following list gives the mapping of the hardware of the DVB-S card. It's focus is on the different functions which can be controlled.

Tuner

Access:

PLL: Address $C2 (I2C of SAA7146A) -> only through I2C repeater of QPSK!

QPSK demodulator: Address $D0 (I2C of SAA7146A)
Address $D1 (I2C of SAA7146A)

	Functions	Controlled by
	Reset	SAA7146A, GPIO2
	LNB on/off	QPSK, OP1
	Polarization	QPSK, OP0
	DiSEqC	QPSK
	Low/high band	QPSK
	Symbolrate	QPSK
	Frequency	PLL
	Others	QPSK
	Infrared	MSP430F1101 -> SAA7146A, GPIO3 for signaling, DEBI read for reading data

The MPEG data from the tuner goes to:
- SAA7146A (D1 port B)
- Common interface (MPEG data in)

The 'decoded' MPEG data from the common interface goes to:
- SAA7146A (D1 port A)

Infrared

To be able to be remote controlled the card has a dedicated microprocessor plus some hardware to receive infrared commands. The microprocessor, the MSP430F1101 (U13), receives the infrared data, decodes it and when valid data is detected it informs the SAA7146A (U5).
Communication between MSP430F1101 and SAA7146A takes place using the DEBI interface of the SAA7146A. When (remote control) data is available the MSP430F1101 activates the GPIO3 line of the SAA7146A. At the same time the data from the MSP430F1101 is latched in the buffer 74LVC574A (U14).
This data from the buffer can then be read using a DEBI read sequence by the SAA7146A.

DEBI read

When a DEBI read sequence is initiated the data appears in the high byte of the data (assuming a 'normal' DEBI transfer has been initiated, thus without byte swapping active). The DEBI transfer must be a '16-bit' cycle (SLAVE16, bit 19 of DEBI_CONFIG should be set active).
When reading from the DEBI interface an address is typically supplied to indicate which device is to be read from the DEBI interface. The infrared device does not have a address decoding mechanism. This means that when data is read from the DEBI interface it will *always* contain infrared data (in the high byte). Note that only reading from *even* addresses is allowed. This is because we are using a 16-bit cycle.
Note: the common interface is also connected to the DEBI interface. When accessing the DEBI interface the common interface data is in the low byte of the data read. For the common interface the address *is* used. The DEBI configuration settings as used for the common interface can be used, except that we need to set the 16-bit cycle. The common interface requires 8-bit cycles! The address typically used to read the infrared data is address $4000.
To handle reception of the infrared data we can either have the GPIO3 line generate an interrupt and then manually read out the data or we can use one of the two available RPS programs of the SAA7146A. An example of such a RPS program (tokenized working example!):

Offset in RPS program (Each 4 bytes)	*Command*	*Comment*
0	RpsPause or RpsGpio3	Wait for GPIO3 being activated
1	RpsLdReg or (DebiCommand shr 2)	Write DEBI command and address to shadow RAM
2	DebiCmdRd or (2 shl 17) or Laddress	'Laddress ' is the address to be accessed, eg $4000
3	RpsClrSignal or RpsDebi	Reset "shadow uploaded" flag
4	RpsNop	
5	RpsUpload or RpsDebi	Invoke shadow upload
6	RpsNop	
7	RpsPause or RpsDebi	Wait for shadow upload to finish
8	RpsStReg or ((DebiAd-4) shr 2)	Get DEBI data (note: -4 correction necessary!!!)
9	– **physical** address of target memory here–	
10	RpsPause or RpsInvert or RpsGpio3	Wait for GPIO3 being de-activated
11	RpsPause or RpsGpio3	Wait for GPIO3 being activated
12	RpsLdReg or (DebiCommand shr 2)	Write DEBI command and address to shadow RAM
13	DebiCmdRd or (2 shl 17) or Laddress	'Laddress ' is the address to be accessed, eg $4000
14	RpsClrSignal or RpsDebi	Reset "shadow uploaded" flag
15	RpsNop	
16	RpsUpload or RpsDebi	Invoke shadow upload
17	RpsNop	
18	RpsPause or RpsDebi	Wait for shadow upload to finish
19	RpsStReg or ((DebiAd-4) shr 2)	Get DEBI data (note: -4 correction necessary!!!)
20	– **physical** address of target memory here, typically 4 higher than first used address–	
21	RpsPause or RpsInvert or RpsGpio3	Wait for GPIO3 being de-activated
22	RpsPause or RpsGpio3	Wait for GPIO3 being activated
23	RpsLdReg or (DebiCommand shr 2)	Write DEBI command and address to shadow RAM
24	DebiCmdRd or (2 shl 17) or Laddress	'Laddress ' is the address to be accessed, eg $4000
25	RpsClrSignal or RpsDebi	Reset "shadow uploaded" flag
26	RpsNop	
27	RpsUpload or RpsDebi	Invoke shadow upload
28	RpsNop	
29	RpsPause or RpsDebi	Wait for shadow upload to finish
30	RpsStReg or ((DebiAd-4) shr 2)	Get DEBI data (note: -4 correction necessary!!!)
31	– **physical** address of target memory here, typically 8 higher than first used address–	
32	RpsPause or RpsInvert or RpsGpio3	Wait for GPIO3 being de-activated
33	RpsJump	Restart program
34	– **physical** address of start RPS program, thus pointing to instruction at offset 0 –	

Note that you need to use the physical addresses here (as you always should in a RPS program). Do not use the virtual addresses. The reason is that different operating systems use these differently. For example; for Windows 98 both virtual and physical addresses are the same, but for Windows XP/2000 virtual and physical addresses are not!
The application only needs to read out the 'target' memory to have access to the data. Alternatively we could have the RPS program issue an interrupt at the end of it's program (just before it jumps back to the start). The application is then to be 'interrupted' when new data is available.
Important: Above code only works if the common interface is not accessed 'simultaneously'. This is because access with the common interface would require a change to 8-bit cycles, instead of 16-bit cycles.

Infrared data

The MSP430F1101 generates three sequences to pass all data to the SAA7146A. Although the order may vary of these three bytes, they can be identified by their contents:

$00 <= Data < $40 -> Device and toggle information
$40 <= Data < $80 -> Command data 1
$C0 <= Data <= $FF -> Command data 2

As can be seen from these three bytes two contain command data. These are the data from the last two detected remote control codes. Only when a key is pressed very shortly these two codes can indicate different commands (this depends on the remote control used). If a remote control is used which repeats a pressed key by default then these two codes indicate the same command.

The MSP430F1101 is programmed to detect RC5 formatted codes only. This format is a well known, widely used, format, which was developed by Philips. The RC5 format contains two types of information: a command and the device for which the command is intended. The MSP430F1101 accepts *all* RC5 commands for *every* device. The *extended* RC5 format is not supported by the MSP430F1101.

Device and toggle information

The device and toggle information are contained in a single byte. In this byte a single bit is used to indicate the toggle situation (the same key is pressed again). Bit 5 is used for this ($20). All the other bits are used to indicate the device code contained in the RC5 message. The device code can range from 0 to 31 ($00..$1F).
Thus:

%xxTDDDDD T = toggle bit
D = device code
Xx = not used

Command data

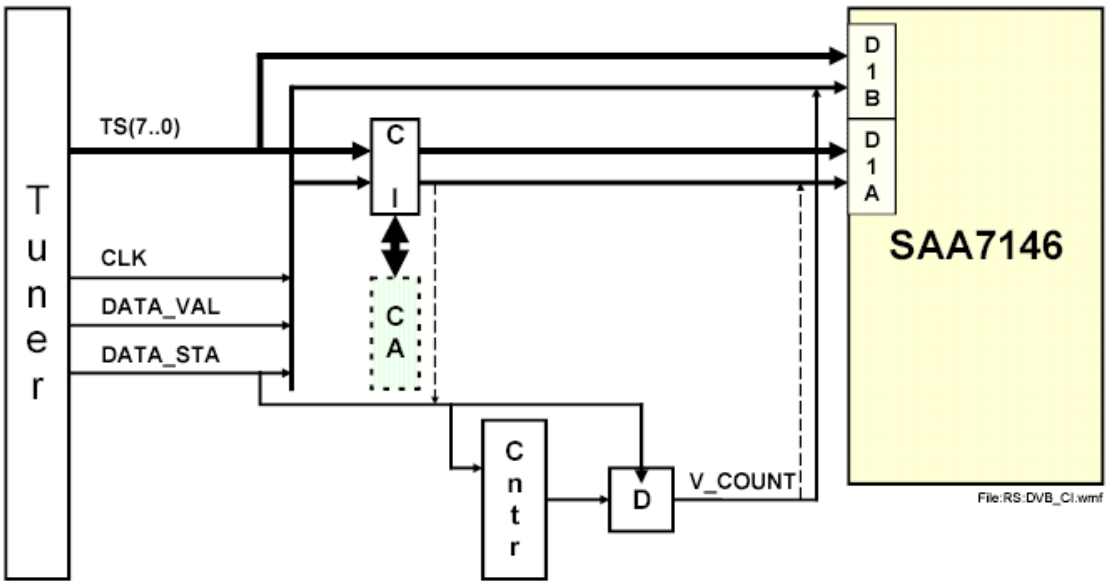
Two bytes are used to contain command data. Although a single byte could suffice, two bytes make it more reliable. Typically these two bytes must indicate the same command to be recognized as valid (this is up to the application). Both bytes are coded differently to indicate if we are handling with the first or second command data.
If we have a value ranging from $40..$7F then we are dealing with command byte 1. We simple subtract $40 to get the command (commands range from 0..63 == $00..$3F).
A value ranging from $C0..$FF indicates the second command. For this we subtract $C0 to get the command.

Transport data stream interface communication between BSRU6-701A and SAA7146A

The tuner BSRU6-701A (U7) outputs the DVB transport stream data onto the B channel of the D1 interface of the SAA7146A (U5). The signals going from the tuner to the SAA7146A are:

Tuner <> SAA7146A signals		
BSRU6-701A	SAA7146A	Description
CLK_OUT	LLC_B	Clock signal, activate for every byte transported
DATA 0..7	D1 port B bit 0..7	Data bits of transported byte
D/P	PXQ_B	Indicates valid data (1) or not (0)
STR_OUT	HS_B	Packet start synchronization Active for one CLK_OUT cycle for every first byte of transport packet
(*)	VS_B	Packet count Toggles every 512 transport packets (*) Besides the direct signals from BSRU6-701A to SAA7146A there is another signal used which is either derived from the CLK_OUT signal of the BSRU6-701A or from the CLK_OUT signal of the common interface J1. This signal is activated for every 512 of these STR_OUT signals. The selection for using the CLK_OUT from the BSRU6-701A or common interface is done with GPIO1 of the SAA7146A ('1'=BSRU6-701A, '0'=common interface).

The picture below (taken from the Philips reference design 'Sylt') shows the situation:



Differences between BSRU6-701A tuner and the SU1278 tuner

Some DVB-S card are provided with a SU1278 tuner instead of the BSRU6-701A (U7) tuner. Beside some hardware differences the main differences in controlling these tuners by software is:

Software tuner differences		
BSRU6-701A	SU1278	Description
$C2	$C0	I2C address write access TSA5059
$C3	$C1	I2C address read access TSA5059
$C0	$20 (950..1250 MHz) $60 (1251..1550 MHz) $A0 (1551..2050 MHz) $E0 (2051..2150 MHz)	Default control register 2 (byte 5) TSA5059 For the SU1278 the charge pump currents also depend on the frequency range.
$51	$50	Default IOCFG register ($0C) STV0299B The BSRU6-701A uses a complemented Q-input (bit 0), whereas the SU1278 does not.
$12	$92	Default AGC1R register ($0F) STV0299B The BSRU6-701A uses a complemented IAGC output (bit 7), whereas the SU1278 does not.

EEPROM

The lower addresses of the 24C16 EEPROM (U6) are used to store some of the settings the SAA7146A (U5) uses to identify itself on the PCI bus. It is accessed by means of the I2C interface and resides at I2C address $A0.
When the SAA7146A is reset (PCI reset) it will read the contents of an I2C EEPROM to fill in some of the PCI configuration space registers. This way certain characteristics of the PCI bridge are variable.

The following table shows the used addresses of the EEPROM:

EEPROM <> PCI address relationship			
EEPROM address	Typical data	PCI configuration space address	Description
$00	$10	$2C	Sub system identifier, eg.: $1003, $1009, $100C, $100F = TTPCline DVB-S budget $4F52 = 'Sylt' board with Alps BSRU6
$01	$0C	$2D	
$02	$13	$2E	Sub system vendor identifier, eg.: $13C2 = 'TechnoTrend' $1131 = 'Philips'
$03	$C2	$2F	
$04	$26	$3C	Maximum latency
$05	$0F	$3D	Minimum granted time

Common interface

The common interface allows the use of an conditional access module.

Communication between the common interface and SAA7146A takes place using the DEBI interface of the SAA7146A.

The following table shows the addresses used for communication with the conditional access module(s):

DEBI addresses common interface

Note: Since not all addresses are always decoded some ghost images may appear.

DEBI address	Access	Name	Description
$0000 ($0xxx)	READ	Status register	Status of the common interface hardware. %xxxxxxx1 = Module is enabled %xxxxxx1x = Transport stream is enabled %xxxx1xxx = Module 0 present (inserted) %xxx1xxxx = Module 1 present (inserted) ?? %xx1xxxxx = Module 2 present (inserted) ?? %x1xxxxxx = Module 3 present (inserted) ??
	WRITE	Control register	Control register of the common interface hardware. %xxxxxxx1 Module enabled %xxxxxxx0 Module disabled (Reset module) The reset should be asserted for about 1 ms. %xxxxxx1x Transport stream enabled %xxxxxx0x Transport stream disabled Typically also set to disabled when the module is being reset. %x1xxxxxx Interrupts 'module free to accept data' (?) enabled %x0xxxxxx Interrupts 'module free to accept data' (?) disabled %1xxxxxxx Interrupts 'module has data available' (?) enabled %0xxxxxxx Interrupts 'module has data available' (?) disabled
$1000-$1FFF			Module 0 (hardware interface register access) Accesses the hardware interface registers of the module (see EN 50221)
$1xx0	R / W	Data register	Register used to transfer data from host <-> module The number of bytes transferred is set by the size registers
$1xx1	READ	Status register	Reports the status of the module %xx0000x1 Read error (length error) %xx00001x Write error (length error) %x10000xx Module is free to accept data %1x0000xx Module has data to send to host
	WRITE	Command register	Controls the transfer between host and module %0000xxx1 Host control; set '1' by the host when starting a write sequence; reset afterwards. %0000xx1x Size write; set '1' to tell the module what buffer size to use; reset after transfer %0000x1xx Size read; request maximum buffer size from module; reset after transfer %00001xxx Reset the interface (does NOT reset the whole module)
$1xx2	R / W	Size register (LS)	Low byte of size of transfer to initiate/initiated
$1xx3	R / W	Size register (MS)	High byte of size of transfer to initiate/initiated
$2000-$2FFF			Module 0 (access type 2)
$3000-$3FFF			Module 0 (access type 0)
$4000 ($4xxx)	READ	Version	This read only register indicates the version number of the common interface hardware. The high nibble has the major version number. The version is typically $A0.
	WRITE	Clear interrupt	Writing to this register clears the interrupts as enabled in address $0000. %x1xxxxx Clear interrupt 'module free to accept data' (?) %1xxxxxxx Clear Interrupt 'module has data available' (?)

$5000-$5FFF			Module 1 (hardware interface register access) Accesses the hardware interface registers of the module (see EN 50221) For address $5xx0..$5xx3 see description $1xx0..$2xx3
$6000-$6FFF			Module 1 (access type 2)
$7000-$7FFF			Module 1 (access type 0)
Note: Above address typically are repeated from address $8000 onwards. If more than 2 modules are supported the addresses below are used to access these modules.			
$9000-$9FFF			Module 2 (hardware interface register access) Accesses the hardware interface registers of the module (see EN 50221) For address $9xx0..$9xx3 see description $1xx0..$2xx3
$A000-$AFFF			Module 2 (access type 2)
$B000-$BFFF			Module 2 (access type 0)
$D000-$DFFF			Module 3 (hardware interface register access) Accesses the hardware interface registers of the module (see EN 50221) For address $Dxx0..$Dxx3 see description $1xx0..$2xx3
$E000-$EFFF			Module 3 (access type 2)
$F000-$FFFF			Module 3 (access type 0)

DEBI read

Unlike the infrared data, which is also accessed by means of the DEBI interface, the DEBI transfer must be an 8-bit cycle. A 16-bit cycle can not be used because the infrared data will always appear in the high byte of the data, making it impossible to read the odd addresses of the common interface.

Typical setting for the DEBI configuration register (DEBI_CONFIG) is:

. 8-bit cycle
. Timeout set to 2 PCI cycles.
. Timeout enabled
. Intel mode
. No byte swapping
. Auto increment